Layout & Verification

PROJECT 6 CE6325 VLSI DESIGN:

Lamin Jammeh NET-ID: DAL852207

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**Design Function:**

The purpose of the design is to make an FIR\_MAC filter that takes an input data and filters it through the different filter taps (orders) by multiplying the input data with the filter coefficients and accumulating the results down to the final output ports.

**Design Specification:**

Filter order: 15

Filter coefficients: [7, 8, 9, 12, 4, 7, 8, 9, 12, 4]

Data\_in size: 8

Data\_out size: 20

PR\_mul and PR\_add: Pipeline registers for multiplication results and addition results respectively

**Data flow through the filter**

A diagram of a diagram

Description automatically generated

**Cells used in the design**

The design comprises a total of twelve cells with one filler cell. These cells were design to build a library each cell passed DRC and LVS check after which a PEX extraction was performed to obtain the netlist files for cell characterization. Each cell was place side by side to have equal height from VDD to GND and from GND to top of NW drw. A LEF file was obtain from the new library to be used with innovus later in the process development.

A screenshot of a video game

Description automatically generatedshow they have

A computer screen shot of a computer screen

Description automatically generated with medium confidence

Synopsys Primlib was used to perform characterization and modeling for each cell. The operating conditions of all the cells were combined to one liberty files with power pins removed.

Synopsys library compiler was used to create a database file. The db file and the original Verilog code for the design were used to obtain the synthesizable Verilog file using Synopsys design vision

The synthesize Verilog file and the LEF file were used in innovus together with the cell library containing all the designed cells to perform the floor-planning, placement, and routing. The schematic and layout file (DEF file) were export out to be used in cadence virtuoso to finish the final design.

**Filter layout:**

A screen shot of a computer screen

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**DRC results showing zero errors:**

A screenshot of a computer

Description automatically generated

**Filter schematic imported from innovus**

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Description automatically generated

**LVS report:**

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